DESIGN AND FABRICATION OF A MICROWAVE VARACTOR

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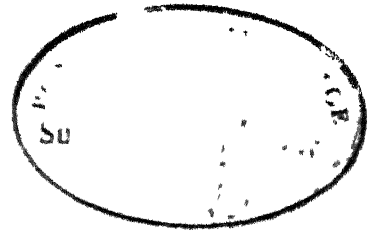
MASTER OF TECHNOLOGY

by

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to the

DEPARTMENT OF ELECTRICAL ENGINEERING

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CERTIFICATE

Certified that this work entitled 'DESIGN AND
FABRICATION OF A MICROWAVE VARACTOR' by Capt AK Nigam has
been carried out under my supervision and has not been
submitted elsewhere for a degree.

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AK NIGAM

ABSTRACT

From the viewpoint of the design of hyperabrupt microwave varactors one needs to know the dependence of the breakdown voltage 'V_B', the capacitance ratio and the cut off frequency 'f_c' as a function of various profile parameters. While designing a varactor for the microwave region the size of the junction achieved and the series resistance of the varactor is also of utmost importance and has to be minimised for achieving higher cutoff frequencies.

The present work was restricted to the design of a single sided hyperabrupt junction microwave varactor for which one side of junction has been assumed to be very heavily doped and on the other side (retrograded region) the impurity concentration has been assumed to be decreasing exponentially with the distance from the junction.

The retrograded region has been designed using two different techniques viz. Double diffusion, and phosphorus diffusion in strong oxidising ambient.

Available plots of the capacitance ratio and the breakdown voltage as a function of surface concentration 'N_o' background to surface concentration ratio 'R_c' and the characteristic length 'Z' have been used for choosing various design parameters.

The breakdown voltage and reverse saturation currents were measured directly from the current-voltage characteristic displayed on the curve tracer. The capacitance, as a function of applied reverse bias, was measured on a Boonton Electronics Corporation, type 74C-518 capacitance bridge which has a fixed test frequency of 100 Kc.

The required breakdown voltage was achieved using double diffusion but could not be achieved using phosphorus diffusion in strong oxidising ambient. The required cutoff frequency also could not be achieved because of nonavailability of epitaxial silicon wafers of required thickness for these particular design parameters. The capacitance ratio of the order of 3.0 w achieved.

LIST OF SYMBOLS

V_B	Breakdown voltage
R_C	Concentration ratio $\left(\frac{N_B}{N_0}\right)$
f_c	cutoff frequency
n	CV index
W_B	Space charge width in retrograded region at breakdown
α_{in}	Ionization rate of electrons
α_{ip}	Ionization rate of holes
N_0	Cross over impurity concentration
W	Space charge width in retrograded region
V_a	Applied voltage across the junction
V_0	Built in voltage of the junction
N_B	Back ground impurity concentration
C	Depletion layer capacitance
A	Junction area
q	Electronic charge
Z	Characteristic length
ϵ	Permitivity of silicon
R_s	Total series resistance of diode
R_j	The leakage resistance
B	Parabolic groth constant for thermal PSG/SiO$_2$ $(cm^2 sec^{-1}$
$X_0(t)$	Oxide thickness at any instant
$N(X,t)$	Depth distribution of phosphorus concentration in silicon at time 't' (cm^{-3})
D	Total width of base region

r   Silicon to SiO_2 volume ratio

D_3 Diffusion coefficient of phosphorus in silicon

m   Segregation coefficient of phosphorus in PSG-Si system

C_o Phosphorus concentration at PSG surface (cm^{-3})

$$= \sqrt{B}/2\sqrt{D_1}$$

L_d Diffusion length

c_3 Capacitance at reverse bias of 3 volts

c_{25} Capacitance at reverse bias of 25 volts

CONTENTS

CHAPTER 1

INTRODUCTION

The variable capacitance diode (also known as Varactor in microwave frequency range) is a P-N junction which is generally used not for its rectifying properties but rather for its voltage dependent reactive properties in reverse bias. The dependence of the depletion layer width and thus depletion layer capacitance on applied voltage can be controlled to suit the intended application by specifying the doping profile through the junction transition region. The only property of junction which is being used in a varactor is the capacitance and thus other facets of the diode are minimised. For using such a diode in microwave frequency range special emphasis is made to reduce all loss elements such as series resistance or fixed reactances which will adversely affect the voltage dependent nature of the diode.

There are many varieties of variable capacitance diodes with most of the differences in characteristics being controlled by differences in doping profile and base thickness relative to the depletion layer width. The two primary modifications in doping profile are concerned with the transition from p-region to the n-region in the formation of the junction. If the doping transition is abrupt in comparison to depletion layer width, then the unit is known as an abrupt junction diode. If the transition is graded in doping throughout the entire excursion

of the depletion layer from zero bias to breakdown, then the unit is known as graded junction.

There can be all sorts of hybrid structures between these two basic forms of junctions or doping profiles, the one in which we are interested is called hyperabrupt junction. In such a diode, the depletion layer continuously moves into a region of lighter and lighter doping as an increasing reverse voltage is applied. As a result the junction capacitance decreases more rapidly than the inverse square root law with voltage exponent reacting as high as five for narrow voltage excursions.

To minimize the losses or resistance associated with the variable capacitance diode the semiconductor substrate or base region must be made as thin as possible, ideally to the extent that the depletion layer at the breakdown voltage extends completely through to the base ohmic junction or contact. This condition of depletion layer extension, which may be termed as 'punch-thru' can be made to occur at reverse voltage considerably less than the breakdown if so desired. Such a Varactor diode exhibits a nearly constant value of capacitance with voltage as the voltage is increased beyond the punch-thru value towards breakdown. Diodes of this type which possess extremel· small losses, are generally more readily fabricated using epitaxial wafers in which the thickness of epitaxial layer (base)

is so choosen that the depletion layer extends to the substrate of lower resistivity at maximum operating voltage.

There are four basic modes of circuit operation employing the variable capacitance diode. The first is the small signal capacitance which is controlled by a reverse bias voltage over an extended range of capacitance change. This mode of operation is basic to all tuning and phase shifting operations where a continuous change in reactance is required and where the RF signal level is very small to cause any reactive change. The second mode of operation is that of switching or providing two impedance states. The third mode of operation is the pumped mode, wherein an RF signal with an appropriate bias is applied to the variable capacitance diode in the reverse bias region to achieve a time-dependent capacitance. This type of operation is employed in all parametric circuits such as amplifiers, converter, or harmonic generators in which the primary source of RF power, namely the pump, is converted into a useful output signal at a new frequency by virtue of the conversion processes obtainable from the nearly loss less time-dependent reactive element. The fourth and final mode of operation is that of power limiting which results from the nonlinear characteristic of the variable capacitance diode such that, as the signal level is increased from a small value to a large one in terms of the applied junction voltage, the impedance level presented by the diode diminishes from some finite capacitive value to a nearly short-circuited state.

For applications in mode one and mode three described above a hyperabrupt junction exhibits a superior characteristic as compared to that of other types of p-n junctions because the former is more voltage sensitive and hence provides a larger capacitance variation and a higher rate of change of capacitance In view of above mentioned applications, the breakdown voltage (V_B) and C-V index (n) are the important parameters of a varactor. The former dominantly determines the range of variable capacitance available and latter, the rate of change of capacitance. Both these parameters solely depend upon the impurity distribution on both the sides of the junctions. However, since we are confining ourself to one sided hyperabrupt junction, therefore, the breakdown voltage and C-V index of a hyperabrupt junction will depend upon the impurity distribution in the retrograded region. As the technology today permits high controllability of impurity distribution, breakdown voltage and C-V* index of a hyperabrupt junction can be pre-determined.

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*C-V Index (n) : The C-V index is defined as the slope of the curve ln C Vs. ln V where C and V are the capacitance of and voltage applied across the junction. It can be expressed as

$$n = \frac{d\ ln(C)}{d\ ln(V)}$$

To relate the device parameters to the details of the impurity profile, we need a programme which can give the optimum values of profile constants for the required device characteristics. As a general approach all the practical profiles for retrograded region could be considered and the one which predicts the best performance choosen.

Different aspects of breakdown in hyperabrupt junctions have been discussed by several authors. AK Gupta and MS Tyagi (1) studied avalanche breakdown voltage of hyperabrupt silicon p-n junctions. Nathanson et al. [2] and M. Shinoda [3] studied avalanche breakdown in silicon hyperabrupt junctions. Various profiles have also been discussed by some authors in detail. Power-law distribution has been investigated [4] by Sukegawa et al. Gaussian profile has been discussed by Kannan et al.[5]. A number of authors have discussed the C-V characteristics of hyperabrupt junctions. A. Shimiju [6] and M. Shinoda [7] calculated the C-V characteristics of hyperabrupt junctions assuming exponential and complementary error function impurity distributions in the retrograded region respectively. Olk [8] has discussed exponential profile as an approximation to the profil obtained by diffusion. The C-V relationships assuming power la distribution in retrograded region have also been derived [9]. For the present work exponential distribution of the impurity concentration has been assumed because of its good approximatic to the impurity profiles obtained by diffusion and also due to its simplicity of analysis.

The other factors, which assumes importance while designing a microwave varactor, are the various losses. These losses prevent the diode from being used as a completely reactive element. The sources of these losses are several, but the most predominant loss is in the base region of the diode. Fig. 1 shows physical and electrical schematic of reverse biased variable capacitance diode. This shows how the remaining portion of the base (N type region) results in the series base resistance R_b. For lower operating voltages this resistance arising due to the undepleted base region is a basic necessity if one is to obtain a variable capacitance diode and can only be minimized by controlling the thickness of the base region with respect to the depletion layer width. If the base width is made sufficiently thin such that the depletion layer extends completely through region to the ohmic contact at the maximum operating voltage then the resistance contributed by this region will vary from some finite value at zero bias to, ideally, a zero value at the maximum operating voltage.

The next most important sources of losses are the series resistances indicated as R_{ps} $\ngtr$ R_{ns} in Fig. 1. R_{ns} is the body resistance of the N^+ or degenerate semiconductor plus the resistance due to contact and R_{ps} is the body resistance of p^+ plus metal contact. Both these sources of series resistance will generally exhibit skin effect and the sum of these resistances at microwave frequencies could be quite significant resulting

in lowering of the Quality factor of variable capacitance diodes. Loss due to $R_J(V)$, representing a conducting loss contributed by bulk and surface leakage through and around the depletion layer could be neglected at UHF range, but at lower frequencies this does become significant and becomes the limiting effect controlling the Q of the varactor.

Finally the package which houses or encapsulates the variable capacitance diode, also, has a pronounced influence on the use of such elements as this will introduce various parasitic elements affecting performance of the diode. Equivalent cct of a encapsulated diode is shown in Fig. 2. Associated with both the capacitive and inductive parasitic elements are losses which can deteriorate the quality of the variable capacitive element. As the current flow in the metallic parts of the package are generally skin effect limited over virtually the entire useful range of this type of device, these parts can contribute losses significant when compared to the losses contained within the semiconductor element itself and therefore must be accounted for when using these elements.

Information regarding the breakdown voltage of exponentially retrograded p^+-n junctions is available in literature [1]. Also the dependence of capacitance ratio (C_3/C_{25}) on different profile parameters, viz., crossover concentration 'N_o', background to surface concentration ration 'R_c' and profile constant 'Z' has

been discussed [10]. In the present work exponentially doped retrograded region has been chosen, which has been formed using different techniques, with an aim to fabricate variable capacitance diodes and to carry out a comparative study of the diodes so formed for use in parametric amplifier.

CHAPTER II

THEORETICAL CONSIDERATIONS

2.0 GENERAL

For the analysis carried out in this chapter, the following assumptions have been made.

(a) The junction considered is one sided p^+-n in which the transition is abrupt and the p-side is so heavily doped that the fermilevel on this side coincides with the upper edge of the valence band.

(b) The impurity distribution in the retrograded n-side decreases exponentially with the distance from the junction.

2.1 THE AVALANCHE BREAKDOWN IN HYPERABRUPT JUNCTION

The expression for impurity concentration in the retrograded junction can be written as (Fig. 3).

$$N(X) = (N_o - N_B) \, e^{-X/Z} + N_B \qquad (2.1)$$

where

X is the distance from the junction

N_o is the cross over impurity concentration at the junction on the retrograded side (i.e. at $X = 0$)

Z is the characteristic length

N_B is the background impurity concentration.

The Poisson's equation for space charge in the retro-graded region, assuming that there are no mobile carriers in the space charge region and also that all the impurity atoms in the space charge region are ionized, can be written as

$$\frac{d^2V}{dX^2} = -\frac{q}{\epsilon} \cdot N(X) \qquad (2.2)$$

Now because most of the voltage drops across the space charge region and also that the electric field due to inhomogeneous impurity distribution in retrograded region is negligible the boundary conditions could be written as

$$V = 0 \quad \text{at} \quad X = 0$$

$$E = 0 \quad \text{at} \quad X = W$$

where

    E is the electric field

    W is width of space charge layer in the retrograded region

Integration of eq. (2.2) with above boundary conditions yields

$$-\frac{dV}{dX} = E(X) = \frac{q}{\epsilon} N_o \left[(1-R_c) \cdot Z \cdot (e^{-\frac{W}{Z}} - e^{-\frac{X}{Z}}) + R_c(X-W) \right] \qquad (2.3)$$

Above equation once integrated with above boundary conditions gives the expression for potential distribution as

$$V(X) = \frac{q}{\epsilon} N_o [(1-R_c)(Z-Zc^{-X/Z} - W e^{-X/Z}) + R_c(X.W - \frac{W^2}{2})] \quad (2.4)$$

from eq. (2.3) and eq. (2.4) expressions for maximum electric field (E_{max}) occurring at X = O and total voltage drop across the junction V(W) can be obtained by putting values of X.

When the electric field in a semiconductor is increased above a critical value (E_{crit}), the carriers gain sufficient energy to generate electron-hole pairs by impact ionization. The generation rate of electron-hole pairs due to impact ionization is

$$G_{np} = \alpha_{in} n \mu_n + \alpha_{ip} p \mu_p \quad (2.5)$$

where

α_{in} is the electron ionization rate ie number of electron-hole pairs generated by an electron per unit distance travelled

α_{ip} is the hole ionization rate due to hole impact

n,p are carrier densities

μ_p, μ_n are carrier mobilities.

Both α_{in} and α_{ip} are strongly dependent upon electric field as follows

$$\alpha_i = A_1 \exp[-(a_i/E)^m] \quad (2.6)$$

where A_1, a_1 and m are constants. The value of m for both electrons and holes is unity. Value of A_1 and a_1 for electrons, in silicon, are 3.80 x 10^6 cm^{-1} and 1.75 x 10^6 V/cm respectively and for holes are 2.25 x 10^7 cm^{-1} and 3.26 x 10^6 V/cm respectively [11].

The threshold condition for avalanche breakdown in a p^+-n junction, where avalanche multiplication is initiated by holes, is given by [11]

$$\int_0^{W_B} \alpha_p \cdot \exp\left[-\int_0^X (\alpha_{ip}-\alpha_{in}) \, dX'\right] dX = 1 \tag{2.7}$$

and the same for an n^+-p junction where avalanche multiplication is initiated by electrons is given by

$$\int_0^{W_B} \alpha_{in} \exp\left[-\int_0^X (\alpha_{in}-\alpha_{ip}) \, dX'\right] dX = 1 \tag{2.8}$$

where

'W_B' is the space charge width in retrograded region at breakdown.

It has been found out that the breakdown field for p^+-n junction is slightly higher [12] than that for n^+-p junction. However, because p^+-n junctions are invariably used in hyper-abrupt Varactors and also because the difference is not very significant only p^+-n junction has been considered here. eq. (2.8) has been solved [1] for W_B for various values of $Z_i R_C$ and

N_o. To obtain the breakdown voltage value of W_B has to be substituted in the expression for $V(W)$. V_B and W_B as a function of N_o with Z as parameter for different values of R_c are plotted in Figs. 3, 4 and 5 [1].

2.2 CAPACITANCE RATIO

The voltage and depletion layer width relation is given by eq. (2.4) which can be rewritten as follows :

$$V(W) = V_a + V_o = \frac{q}{\epsilon} N_o Z^2 [(1-R_c) \{1-(1+ \frac{W}{Z}) e^{-W/Z}\} - \frac{R_c}{2} (W/Z)^2]$$
(2.9)

the depletion region capacitance 'C' can be written as

$$C = \frac{\epsilon}{W} \cdot A$$
(2.10)

where A is the junction area.

eq. (2.9) has been solved [10] iteratively and C_3/C_{25} calculated for different values of R_c and Z at different values of N_o. It was found that $(C_3/C_{25})_{max}$ did not depend on the value of 'Z' for a given R_c and it occurred at the same value of N_o, at a given 'Z' for different values or R_c. Fig. 7 shows a plot between $(C_3/C_{25})_{max}$ and R_c [10] and in Fig. 8 Z_{opt} (defined as the value of Z at which maximum of (C_3/C_{25}) occurs for a given value of N_o) has been plotted against N_o.

2.3 Q VALUE AND CUTOFF FREQUENCY

The small signal equivalent cct of varactor, neglecting
lead inductance and package capacitance, is the parallel combina-
tion of the junction 'C' and the leakage resistance $R_J(V)$ in
series with the total series resistance 'R_s' of the diode. At
high frequencies, such that $R_s \gg \frac{1}{\omega_C}$ the Q of the varactor is

$$Q = \frac{1}{\omega C \ R_s} \qquad (2.11)$$

The cut off frequency 'f_c' of a varactor is defined as the
frequency at which Q = 1, i.e.,

$$f_c = \frac{1}{2\pi C R_s} \qquad (2.12)$$

Now f_c, as well as Q, are functions of the voltage V_a
applied across the junction. The variation of Q with voltage
at high frequencies is usually represented in a Smith chart.
The impedance of the varactor as a frequency ω is given by

$$Z(V) = R_s + \frac{1}{j\omega C(V)}$$

In varactor measurements using the match method [13] it
is customary to match the varactor to the line at zero bias. In
this manner, the impedance of the varactor becomes normalised to
the line or guide impedance such that at Zerobias the series
resistance becomes unity and the reactance zero, thus, the nor-
malised matched varactor impedance becomes

$$Z(V) = \gamma_s - \frac{1}{\omega Z_o}\left[\frac{1}{C(V)} - \frac{1}{C(O)}\right] \quad \text{or,}$$

$$= r_s - \frac{J}{\omega C(O)Z_o}\left[\frac{C(O)}{C(V)} - 1\right] \tag{2.13}$$

where the net reactance at zero bias equals zero and $r_s(O) = \frac{R_s}{Z_o} = 1.$

It is interesting to note that the cutoff frequency as defined by eq. (2.12) is also dependent on the material. For instance for the case of an abrupt P^+NN^+ varactor, the value of R_s can be taken as the resistance of the base region. In this case the cutoff frequency is given by

$$f_c = \frac{q\mu N_B W}{2\pi\epsilon(D-W)} \cong \frac{q\mu N_B W}{2\pi\epsilon D} \tag{2.14}$$

where W is the depletion layer width given by

$$W = \left(\frac{2\epsilon}{qN_B} V_{(W)}\right)^{1/2} \tag{2.15}$$

Equation (2.14) can be written as

$$f_c = \frac{\mu}{\pi D}\left(\frac{q}{2\epsilon}\right)^{1/2}\left\{N_B V_{(W)}\right\}^{1/2} \tag{2.16}$$

eq. (2.16) shows that the cut off frequency at a given bias is dependent upon N_B, V(W) and the thickness of the base region. This is understandable because with increasing N_B the decrease

in the base resistance is more pronounced as compared to the increase in the junction capacitance. Also the minimum thickness of the epilayer and maximum value of N_β, compatible with breakdown voltage, should be choosen to get the maximum cut off frequency.

CHAPTER III

FORMATION OF RETROGRADED REGION

3.0 DIFFUSION TECHNIQUE

To form the retrograded region diffusion process is to be carried out, for which, it is necessary to bring an external phase containing the diffusant into contact with the semiconductor at an elevated temperature and for diffusion to take place there should be correct vapour pressure surrounding the semiconductor material. If the pressure is greater than its equilibrium pressure, then solute atoms will leave the vapour phase to join the crystal lattice, and if the pressure is less than equilibrium pressure, the dopant will leave the solid phase, The most suitable diffusion method depends partly on the diffusion system and partly on the intention of the experiment. If the main purpose of the diffusion is to elicit information on the diffusion mechanism, then it is preferable to have it take place in a sealed ampoule containing known amounts of semiconductor and diffusant. The ampoule then becomes a system about which everything is known and various theories of semiconductor solutions could be used to find out the parameters.But if the intention is to use the diffusion process to prepare no. of samples then the sealed-tube method becomes impractical because the business of sealing off an ampoule at the start of

every experiment and breaking it at the end is too much trouble
and a constant-flow method becomes important. In this method
the diffusant enters one end of a long tube as a vapour, flows
over the semiconductor and leaves at the other end. Due to
its simplicity and ease the later method has been used for
present work. To form retrograded/various diffusion techniques
could be utilised each technique has its limitations and advan-
tages. Conventional system employing open tube diffusion leads
to very high surface concentration because of large segregation
coefficient of phosphorus and it is difficult to get concentra-
tion below $10^{19}/cm^3$ [14]. Diffusion through intermediate oxide
layer [15] poses problems of reproducibility, slight change in
the density, quality or the thickness of the intervening oxide
layer drastically affects the concentration at the silicon sur-
face. Doped oxide [5] source needs an elaborate set up and
requires time to standardize the whole process. For the present
work three different techniques were tried, the first was that
of two step diffusion followed by etching of the top highly
doped surface layer. This method requires an accurate and
uniform etching of the surface and slight difference in the
etching rate can cause a large fluctuation in the value of N_o
and hence a etchant with slow etching rate is preferable. This
method, inspite of its limitations, was used because of its
simplicity and ease. The second method used the diluted phospho-
silica film spun on the silicon surface as the source, but it

was found that at the diffusion temp of $1100^\circ C$ and above it
formed a compound on the surface of silicon which could not be
removed and hence this method was discarded. Phosphorus diffu-
sion in strong oxidising ambient [16] was tried next to achieve
low surface concentration required for formation of retro-
graded region.

3.1 DOUBLE DIFFUSION

When diffusion from the vapour phase takes place at a
temperature close to the melting point of the semiconductor
crystal, evaporation from the crystal can occur on quite a
large scale. Any crystal will require a vapour pressure of its
own elements, to be in equilibrium at a high temperature. If
the diffusion takes place in a closed vessel, the crystal will
evaporate until the correct vapour pressure has been built up.
In open systems, which has been used here, the evaporating
material will tend to be carried away by the flow of the vapour,
and the required vapour pressure may not be achieved. In such a
case the crystal will continue to evaporate and thus the surface
of the crystal will be moving with a finite velocity with res-
pect to rigid frame of reference. This problem of diffusion has
been solved by Kucher [17] and the profile has the following
form

$$N(X) = \frac{N_o'}{2} \left(\text{erfc} \frac{X+vt}{2(Dt)^{1/2}} + \exp - \frac{vX}{D} \text{erfc} \frac{X-vt}{2(Dt)^{1/2}} \right) \qquad (3.0)$$

where N_o' is the equilibrium concentration at the moving interface

t is the time for diffusion, v the velocity of the moving interface and D is the diffusion coefficient.

If the temp is low compared to the melting point of the semiconductor material then the velocity $\rightarrow 0$ and above eq. reduces to

$$N(X) = \frac{N_o'}{2} \operatorname{erfc} \frac{X}{2(Dt)^{1/2}} \qquad (3.1)$$

For predeposition in a double diffusion method the above approximation has been used but this places a upper limit for the diffusion temperature. For silicon this approximation can be safely used upto diffusion temp. of $1200^\circ C$. The drive in could be at high temperature which results in a Gaussian-type profile. The resulting impurity profile of these two steps lies between the corresponding erfc and Gaussian profiles and is a function of diffusion conditions. A more erfc like distribution if $D_p t_p \gg D_d t_d$ and more Gaussian-like distribution if $D_p t_p \ll D_d t_d$, where,

D_p - Diffusion coefficient at predeposition temp.

D_d - Diffusion coefficient at drive in temp.

t_p - Predeposition time

t_d - Drive in time

The actual impurity profile can be described by

$$[N(X,t_p,t_d)+N_B]/N_{SD} = \tan D_1 \cdot \int_{u=0}^{D_1} \exp[-(X^2/4D_2)(1+U^2)]/(1+U^2)\,d\psi$$

(3.2)

where

$N_{sd} = (2/\pi)\, N_{sp}/\tan D_1 =$ the final surface conc after drive-in

$N_{sp} =$ surface conc after the first diffusion

$D_1 = (D_p t_p\, D_d t_d)^{1/2}$

$D_2 = D_p t_p + D_d t_d$

Several plots are available in literature giving the impurity profile as a function of various parameters.

3.2 PHOSPHORUS DIFFUSION IN STRONG OXIDISING AMBIENT

The impurity concentration distribution in silicon under strong oxidizing ambient and assuming a constant source diffusion and parabolic oxide growth is given by [16]

$$N(X,t) = A \cdot \mathrm{erfc}\left[\frac{Z+r\sqrt{Bt}}{2\sqrt{D_3 t}}\right]$$

(3.3)

where

$$A \quad \frac{mC_o}{1 + \sqrt{\pi}\,\delta\, e^{\varsigma^2}\, \mathrm{erfc}(\varsigma)\; F\; \frac{r\sqrt{B}}{2\sqrt{D_3}}}$$

(3.4)

$$F\left(\frac{r\sqrt{B}}{2\sqrt{D_3}}\right) = 1+mr\left[\cfrac{1}{\sqrt{\pi}\left(\frac{r\sqrt{B}}{2\sqrt{D_3}}\,e^{r^2 B/4D_2}\,\text{erfc}\left(\frac{r\sqrt{B}}{2\sqrt{D_3}}\right)^{-1}\right)}\right] \qquad (3.5)$$

The impurity concentration at silicon surface is given by

$$N(o,t) = A\cdot\text{erfc}\left(\frac{r\sqrt{B}}{2\sqrt{D_3}}\right) \qquad (3.6)$$

According to eq. (3.4), the value of 'A' can be varied by orders of magnitude simply by varying 'B' i.e.the oxidation rate for the same value of C_o i.e.constant dopant concentration in the diffusion ambient. The oxidation rate can be controlled by controlling the partial pressure of oxygen in the ambient. For achieving a low surface concentration large values of (high oxidations rate) and D_3 (high diffusion temperature) are desirable.

CHAPTER IV

DEVICE FABRICATION AND MEASUREMENTS

4.0 DESIGN CONSIDERATIONS

While designing a microwave varactor a compromise between various parameters has to be reached to get best results. It is evident from Figs. 4,5 and 6 that for same values of N_o different values of breakdown voltage and depletion layer width at breakdown voltage will be achieved. It was decided to design a variable capacitance diode with a capacitance ratio of 5 with a breakdown voltage of 30 volts capable of operating in microwave range. Taking into account various variations and experimental errors the design was aimed to achieve a capacitance ratio of 6's breakdown voltage of 40 volts.

From Fig. 7 we see that required value of $R_c \leq 0.5$ and from Fig. 5 we see that various combination of N_o and Z values can be used. It was decided to choose $N_o = 8 \times 10^{16}$ and Z = 0.5364 which will give desired breakdown voltage and the depletion layer width at breakdown to be approximately 3μ. Fig. 8 gives optimum value of 'Z' to be .17μ but this would give a too large value of depletion layer width at breakdown thereby reducing the cut off frequency. The required N_B thus calculated was $N_B = 4 \times 10^{15}$ which corresponds to resistivity of 1.5 Ω cm.

4.1 FABRICATION PROCESS

4.1.1 Sample Preparation

The samples used in the experimental work were n-type and n on n^+ epitaxial silicon wafers. The epitaxial layer thickness was 6μ and thickness of the samples was varying from 9 to11 mils. The conductivity of n wafers was $3-7\Omega$ cm and that of epitaxial wafer was 1Ω cm. One side of these samples was mirror polished and other side lapped. For cutting the wafer it was loaded on the sample holder with front surface downwards on black wax. To cut the wafer the speed of the wire was slowly increased to the reading of 20 on the scale, during cutting it was ensured that a continuous supply of slurry (silicon carbide+ glycerine) it maintained which aids easy and fast cutting.

The samples so obtained were rubbed by tissue paper soaked in Trichloroethylene (TCE) to remove excess of black wax. These samples were then boiled in TCE first for two minutes and then for five minutes to remove any traces of TCE.

Each sample was now processed separately. For prediffusion cleaning hydrogen peroxide (H_2O_2) based cleaning solution [18] was used. Various steps are as follows :

The sample was again boiled in TCE for 5 minutes to remove any grease which might be sticking to the sample. Now the TCE was poured out from the beaker containing the sample and it was

placed on the hot plate till the time left over TCE is evaporated completely, this process will remove any grease sticking to the sample.

The sample now was heated in Acetone followed by heating in Methanol each for five minutes. This removes all the solvents used in previous steps. These steps should be strictly adhered to the sequence given here because solvents of previous steps are removed in following step.

Organic contaminats and metallic contaminants were removed by boiling the sample, after it has been thoroughly rinsed in deionized (DI) water, in H_2O_2: NH_4OH: H_2O::2:1:7 by volume solution and H_2O_2:Hcl:H_2O::1:1:5 by volume solutions respectively for 15 minutes each. Use of metallic tweezers was kept to minimum during entire cleaning operation which could cause deposition of contamination and the sample was thoroughly rinsed in DI water after each cleaning step as an added precaution.

At the end of the above process a thin film of SiO_2 is left on the surface of silicon and was removed by dipping the sample in Buffered HF, is HF:NH_4F::1:10 by volume, for about 30 seconds. While treating the water with BHF (Buffered HF) use of teflon tweezers and beakers was made throughout the experiment.

To remove any traces of metallic contamination the sample was boiled in Conc HNO_3 for about 10 ninutes after thoroughly rinsing it in the DI water. This again forms a thin layer of

SiO_2 and removes any metallic contaminants. The sample was again treated with BHF to remove SiO_2 layer after rinsing thoroughly in DI water. Now the sample should become hydrophobic, if it is not, the last step should be repeated till it becomes hydrophobic.

4.1.2 Two Step Phosphorus Diffusion

Phosphorus diffusion was carried out in two steps for formation of retrograded region. The first step was predeposition which was carried out for 10 minutes at a temp of $950^{o}C$ during this oxygen flow rate was maintained at 40 CC/min, source Nitrogen rate, which was used to bubble the $POCl_3$, was kept at 15 CC/min and the carrier Nitrogen flow rate was maintained at 350 CC/min. This diffusion was expected to give surface conc of $7x10^{20}$ atoms/cm^{-3} being the solid solubility at this temperature. This was followed by drive in diffusion for 35 minutes at a temperature of $1100^{o}C$. The surface conc and the diffusion length at the end of this step was calculated to be $2.3x10^{19}$ atoms/cm^3 and .536 µm respectively. As this surface conc was too high the sample was etched out to remove the top highly doped layer,a conc of $8x10^{16}$ cm^{-3} was calculated to be at a depth of 1.2715 µm and conc of $2x10^{17}$ cm^{-3} was calculated to be at a depth of 1.164 µm. To etch out the samples a special ething solution, with a low etch rate, of $K_2Cr_2O_7$, 5g, and Na_2SO_4 (anhydrous) 2.5 gm and 10 ml. of HF (49%) dissolved in DI water and diluted to

100 ml [19] was used. The etch rate of this solution remains constant at about 1.72 μm/min upto phosphorus doping of 2×10^{18} cm^{-3} and after this increases slowly. To achieve desired surface conc two samples were etched in this solution for 40 sec and 45 sec respectively. The expected surface conc was 2×10^{17} cm^{-3} and 8×10^{16} cm^{-3} respectively.

4.1.3 Formation of p$^+$ Region

Boron diffusion was used for formation of p$^+$ region. For this Boron Nitride wafers were used as source. Before carrying out diffusion the Boron Nitride wafer was oxidised at 900°C for 20 minutes after cleaning it in 10% HF for 10 sec followed by ultrasonic cleaning in DI water for two minutes. The oxygen flow rate for oxidation was maintained at 200 CC/min. The sample was now loaded for p-type diffusion. Since the junctions were required to be shallow p$^+$-n type, only deposition was carried out at 950°C for 20 minutes with nitrogen rate of 550 CC/min. The expected surface conc was of the order of 3.5×10^{20} cm^{-3} being solid solubility at that temp.

4.1.4 MESA Etching

A layer of apiezon wax was used to protect the surface of p$^+$ side and the back side of the wafer. For this a thick solution of apiezon wax was made in TCE and small dots of this solution were put on the p$^+$ side with the help of a syringe.

The unpolished side of the wafer was also completely protected by same solution. The etching solution used was $HF:HNO_3:CH_3COOH$ ::1:8:1 by volume. The etching rate of this solution was measured to be 5.2 micron/min. Etching was done for 5 minutes and the measured MESA height was found to be one mil.

4.1.5 Ohmic Contact

The sample, after the MESA structure were formed, was boiled in TCE till the time any traces of black wax were removed. It was considered necessary to protect top surface by thick apiezon solution before final nickel plating was done, because for the initial runs it was observed the nickel plating was done on the front surface too thereby shorting the diodes. The unpolished back side of the wafer was lapped with 9 micron Al_2O_3 powder so as to remove the p-diffused layer completely. Ohmic contact, to this side, was made by electroless nickle plating [20]. The front side being very heavily doped is expected to provide a good ohmic contact to the metal probes.

4.1.6 Phosphorus Diffusion in Strong Oxidizing Ambient

Phosphorus Diffusion in strong oxidizing ambient was used to form the retrograded region for second set of diodes. The diffusion time was kept one hour and diffusion temperature was kept $1100^{o}C$. The flow rates of oxygen and $N_2/POCl_3$ were kept at 640 CC/min and 14.5 CC/min [21]. Formation of p^{+} region, MESA structures and ohmic contacts was done as already explained.

4.2   MEASUREMENTS

The I-V characteristic of the junctions was directly displayed on the curve tracer and the breakdown voltage was determined.

The capacitance measurement were taken on a Boonton Electronics Corporation, type 74C-S18 capacitance bridge. This bridge is a fixed frequency (100 KC) bridge which reads an accuracy of .25 percent in absence of any shunt conductance.

CHAPTER V

RESULTS AND DISCUSSION

5.0 JUNCTIONS FORMED USING PHOSPHORUS DIFFUSION IN STRONG

OXIDIZING AMBIENT

Most of the junctions formed using this method showed a
breakdown voltage of less than ten volts. This suggests that
the surface concentration achieved was more than expected.
Formation of retrograded region using phosphorus diffusion in
strong oxidizing ambient needs further experimental work to
standardize the complete process to achieve low surface con-
centration.

5.1 JUNCTIONS FORMED USING DOUBLE DIFFUSION

Junctions formed on sample one, which was etched for less
time, showed breakdown voltage of about 30 Volts for most of
the diodes and for junctions formed   on sample two, which
was etched for more time, showed higher breakdown voltage. The
higher breakdown voltages achieved could be attributed to lower
values of N_o achieved for both the cases. This may be due to
deeper diffusion of the p^+-layer using boron nitride source and
also due to the higher etch rate of etching solution used to
etch the top heavily doped surface of samples.

The series resistance of the diodes for both the samples was found to be quite high which was of the order of 150 Ω for most of the diodes. The high values of resistance obtained could be attributed to the use of nonepitaxial wafers. As the depletion layer extends to few micron thickness only most of the n region of the wafers acts as series resistance and in addition there is contact resistance of nickel on the wafer.

The capacitance values obtained are quite large and can be controlled by using photolithographic techniques and use of masks of proper size.

From the plots of Fig (10) and (11) it is seen that hyperabrupt nature of the junction is displayed only for narrow voltage excursions and also the capacitance ratio obtained is about 3.0 instead of 6 for which the diode was designed.

Further work needs to be done to get hyperabrupt nature of the junction for large voltage excursions which can be of use for application in parametric amplifier or any other such device.

CHAPTER V

CONCLUSION

Available plots have been used for the present work to obtain the optimum values of the profile parameters N_o, R_c and Z for the formation of the retrograded region of a one sided hyperabrupt variable capacitance diode. Open tube diffusion method was used for the work which is most suited for the experimental works.

To form the retrograded region three different diffusion techniques were used. Diffusion from a thin layer of diluted phosphosilica film, which was spun on the surface of the silicon wafer, was not successful as it formed an insoluble compound on the silicon surface at diffusion temperature. At lower temperature it was found that no such compound was formed but the reverse saturation current for the junction so formed was quite large. The technique next tried was the phosphorus diffusion in strong oxidizing ambient which gave low breakdown voltages.

The first sample formed using double diffusion technique gave a breakdown voltage of approx 30 volts for most of the junctions as against about 12V calculated using plots. The second sample, which was etched for more time gave breakdown

voltage of more than 40 volts. Greater breakdown voltage for both the cases could be attributed to the deep diffusion of the p^+ region and to the higher etching rate of the etching solution.

Expected cut off frequency of the diodes was expected to be quite low due to the use of nonepitaxial wafers. The series resistance of the diodes was also very/which again is due to the use of non epitaxial wafer and the large contact resistance of nickel with silicon. For application of the variable capacitance diodes in the microwave frequency range the series resistance has to be further reduced considerably and further work needs to be done to reduce it to the order of few ohms. The capacitance achieved in these particular runs was found to be very high which was mainly due to large junction area of the diodes. Use of photolithographic techniques with proper mask size will, however, give desired capacitance values.

Phosphorus diffusion in strong oxidizing ambient, though unsuccessful for the present work, is regarded as a better method for forming retrograded region because of its apparent advantages of better controls and reduced processing steps. Further work needs to be done to standardize the complete process to achieve desired surface concentration using this technique.

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METAL CONTACT

P+

R_{ps}

$C_j(V)$ $R_j(V)$

$W(V)$

DEPLETION
LAYER
CREATING
DIODE
CAPACITANCE

N

$R_b(V)$ $C_b(M)$

REMAINING PORTION
OF BASE REGION
CONTRIBUTING
PRIMARY
RESISTANCE

N+

R_{hs}

METAL CONTACT

PHYSICAL
DEVICE

ELECTRICAL
EQUIVALENT

Fig 1

METAL
ENDS

METAL
STRAP
OR
MESH

VARACTOR
ELEMENT

CERAMIC
OR QUARTZ
CASING

MOUNTING
POST
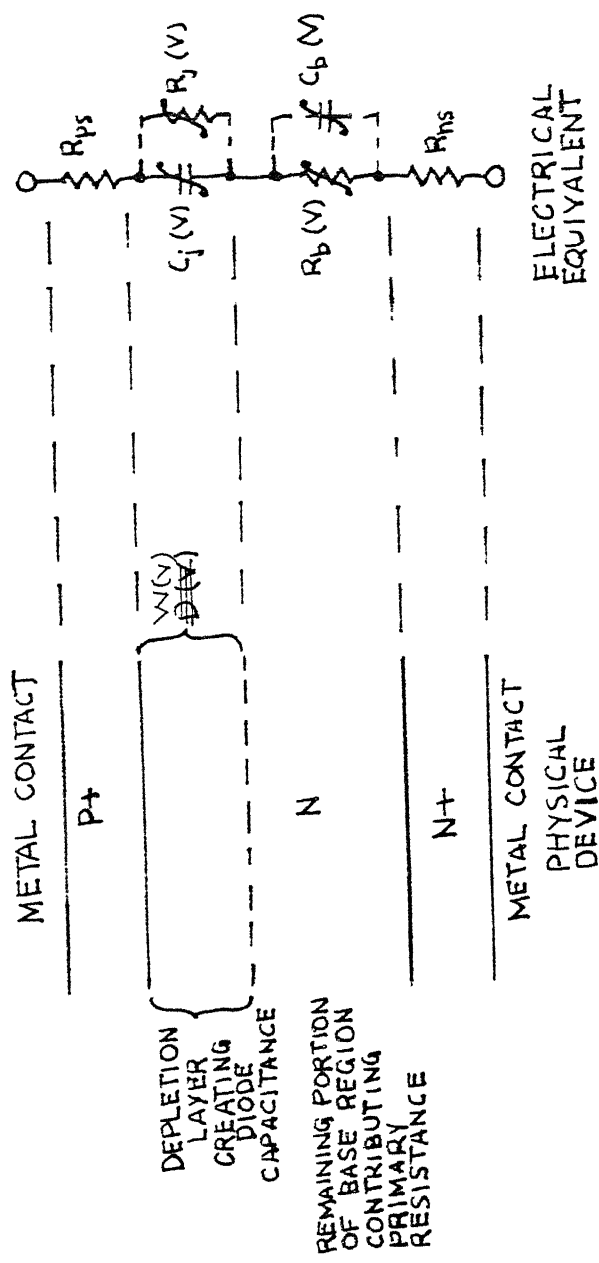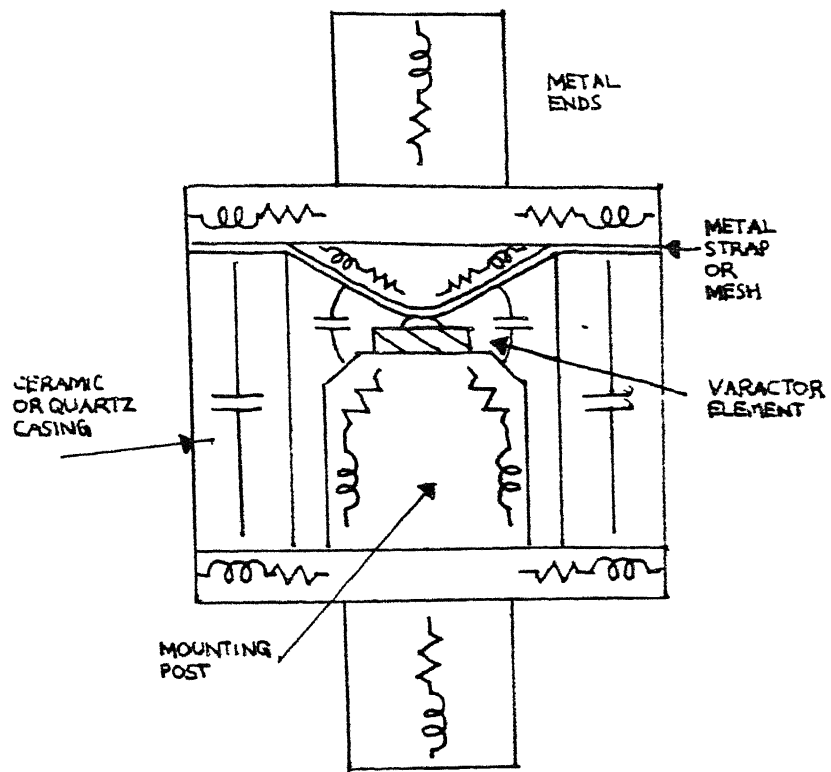
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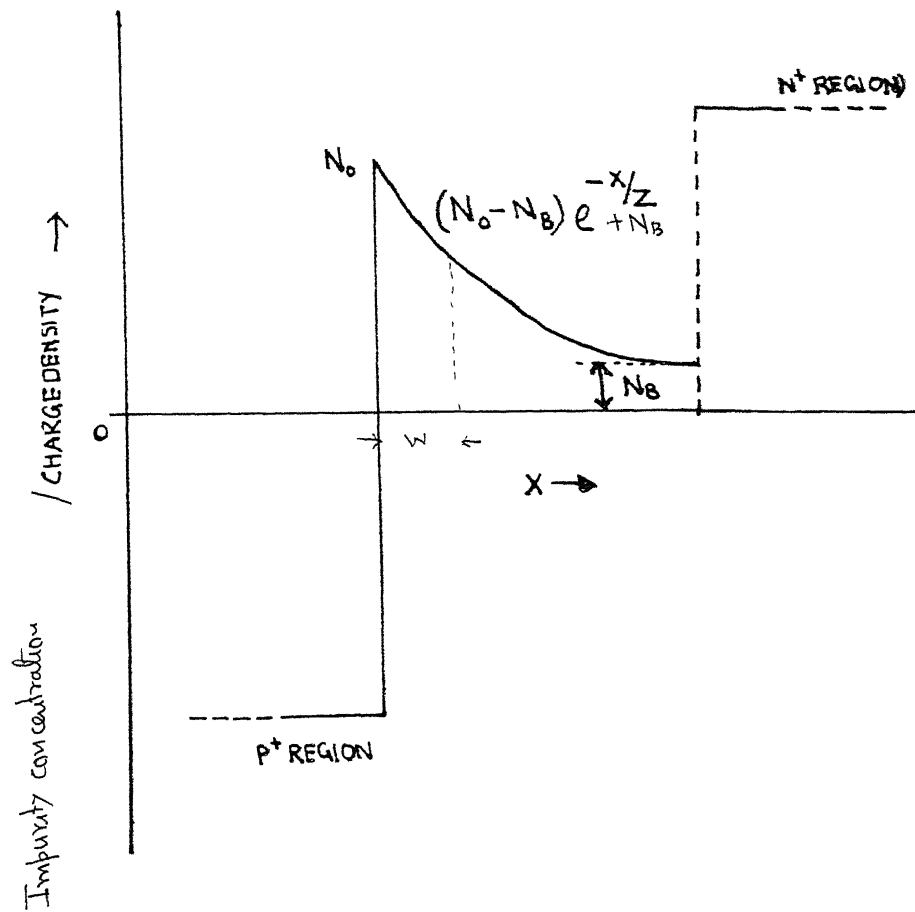
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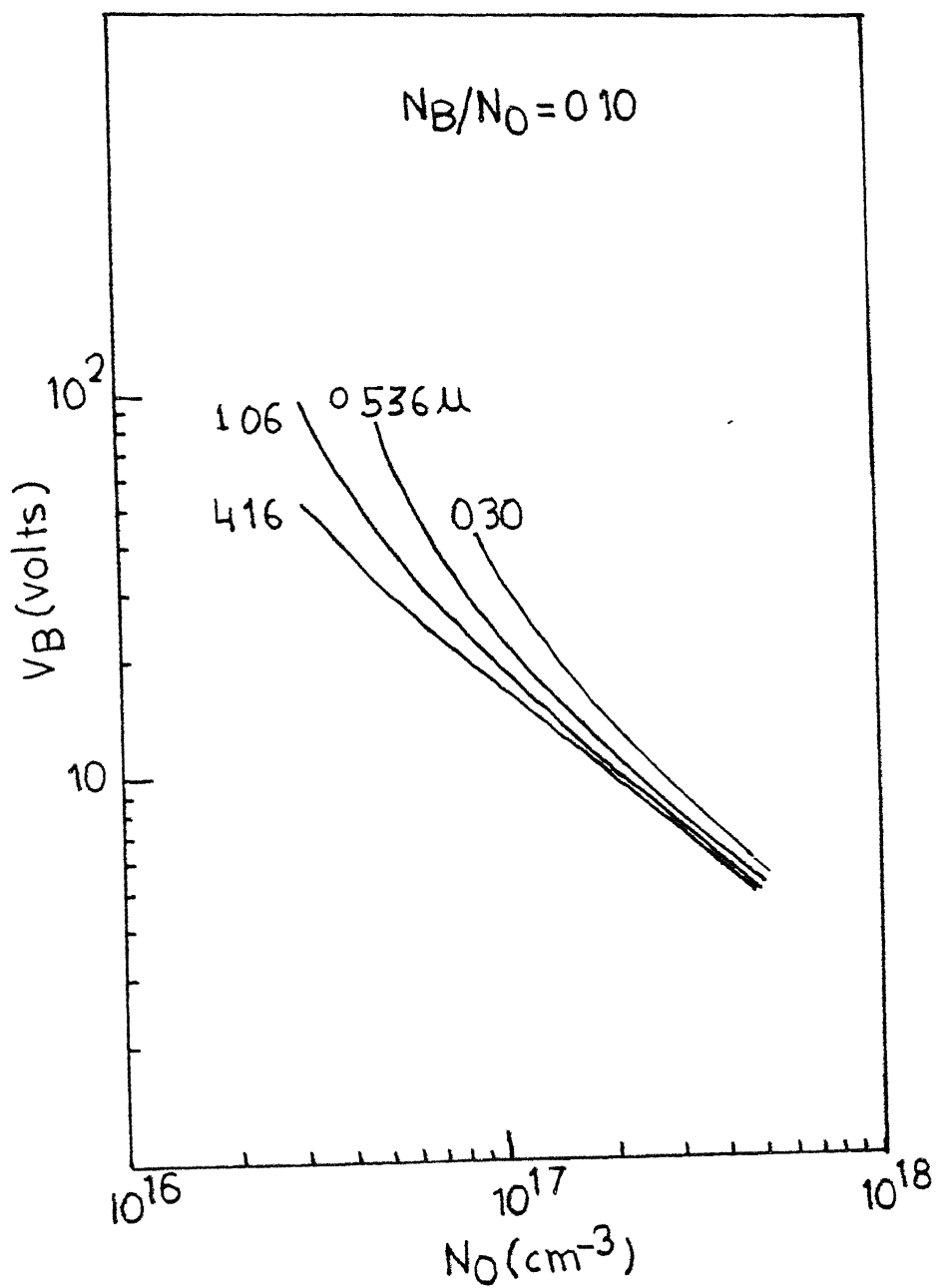
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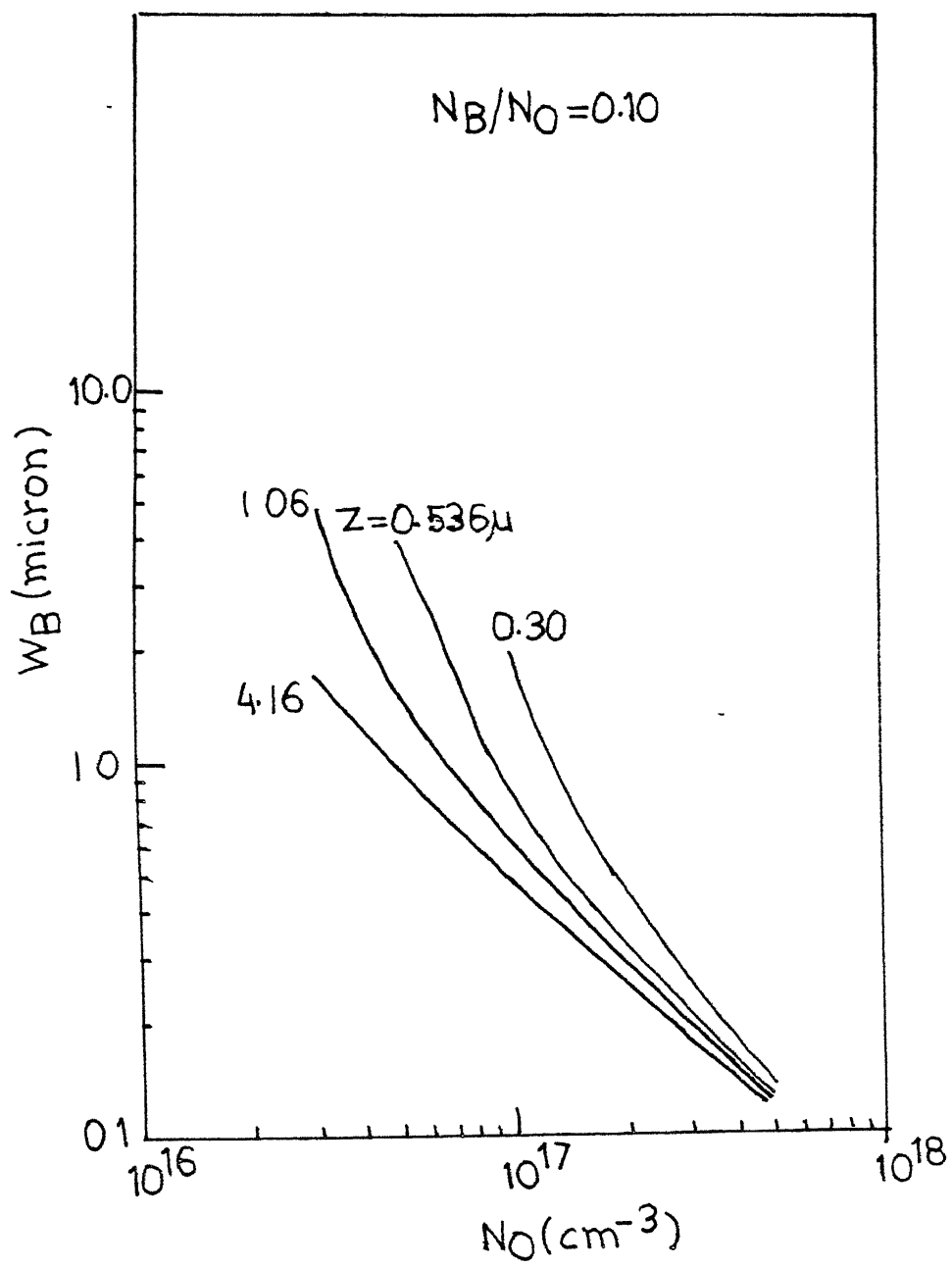
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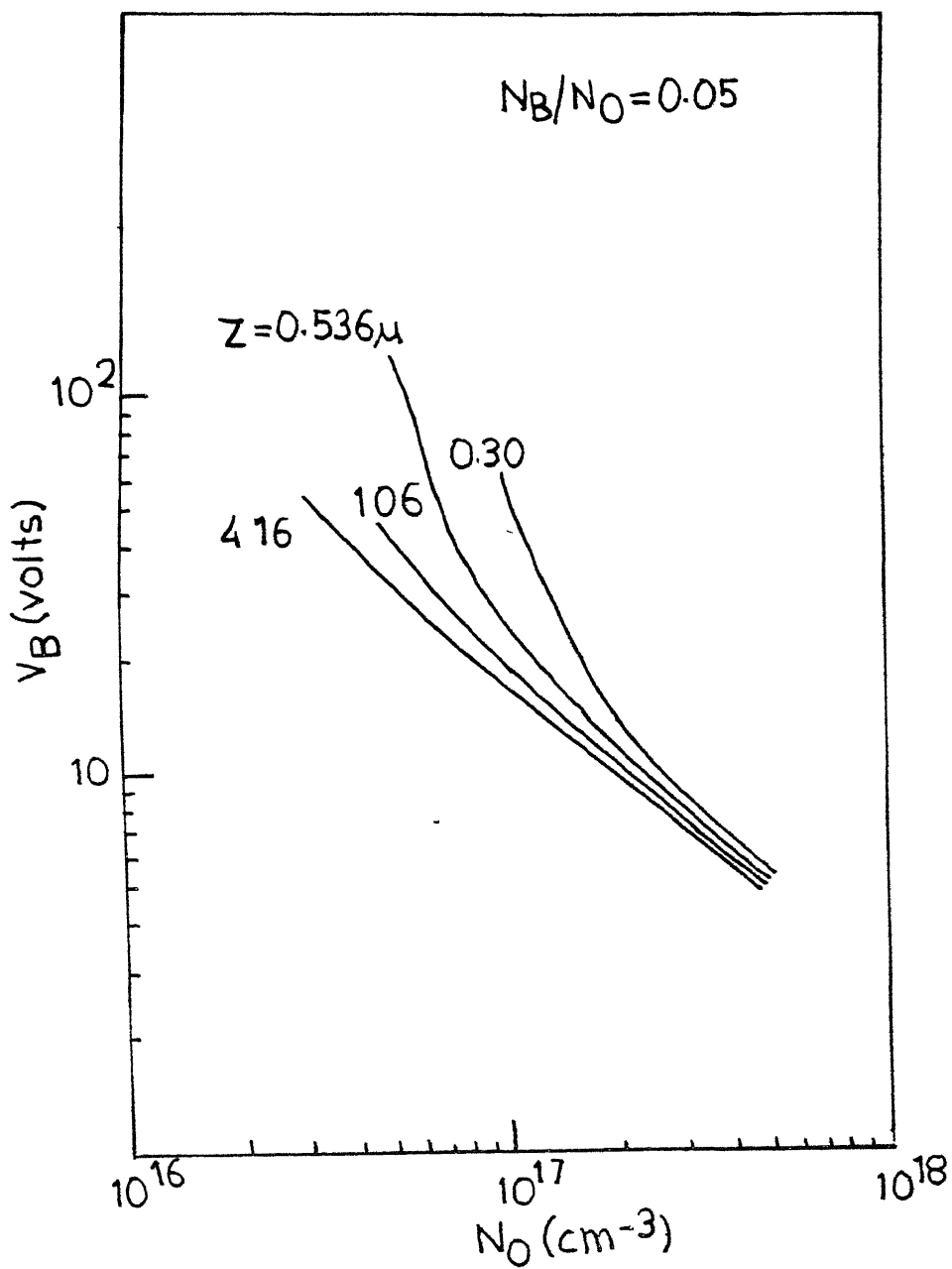
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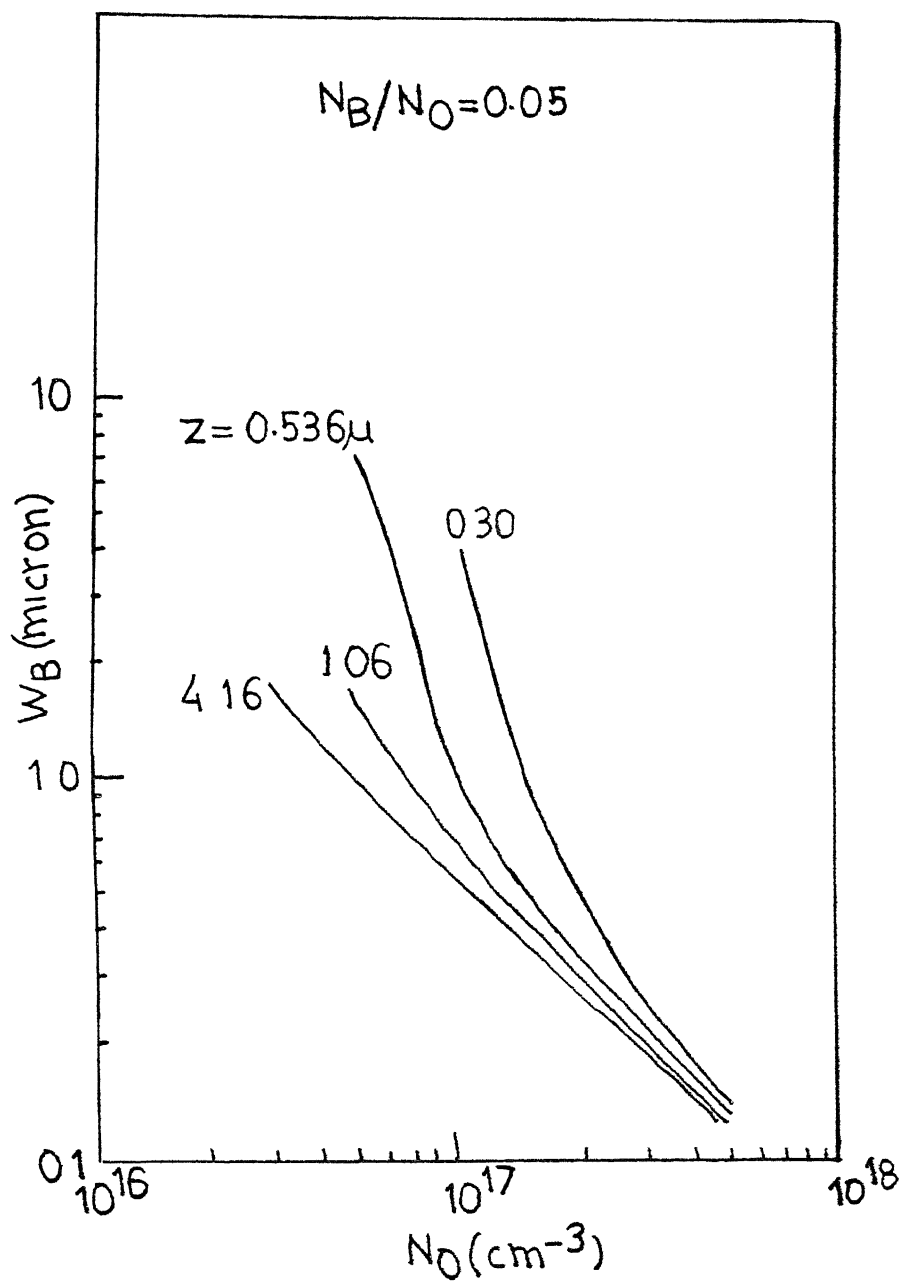
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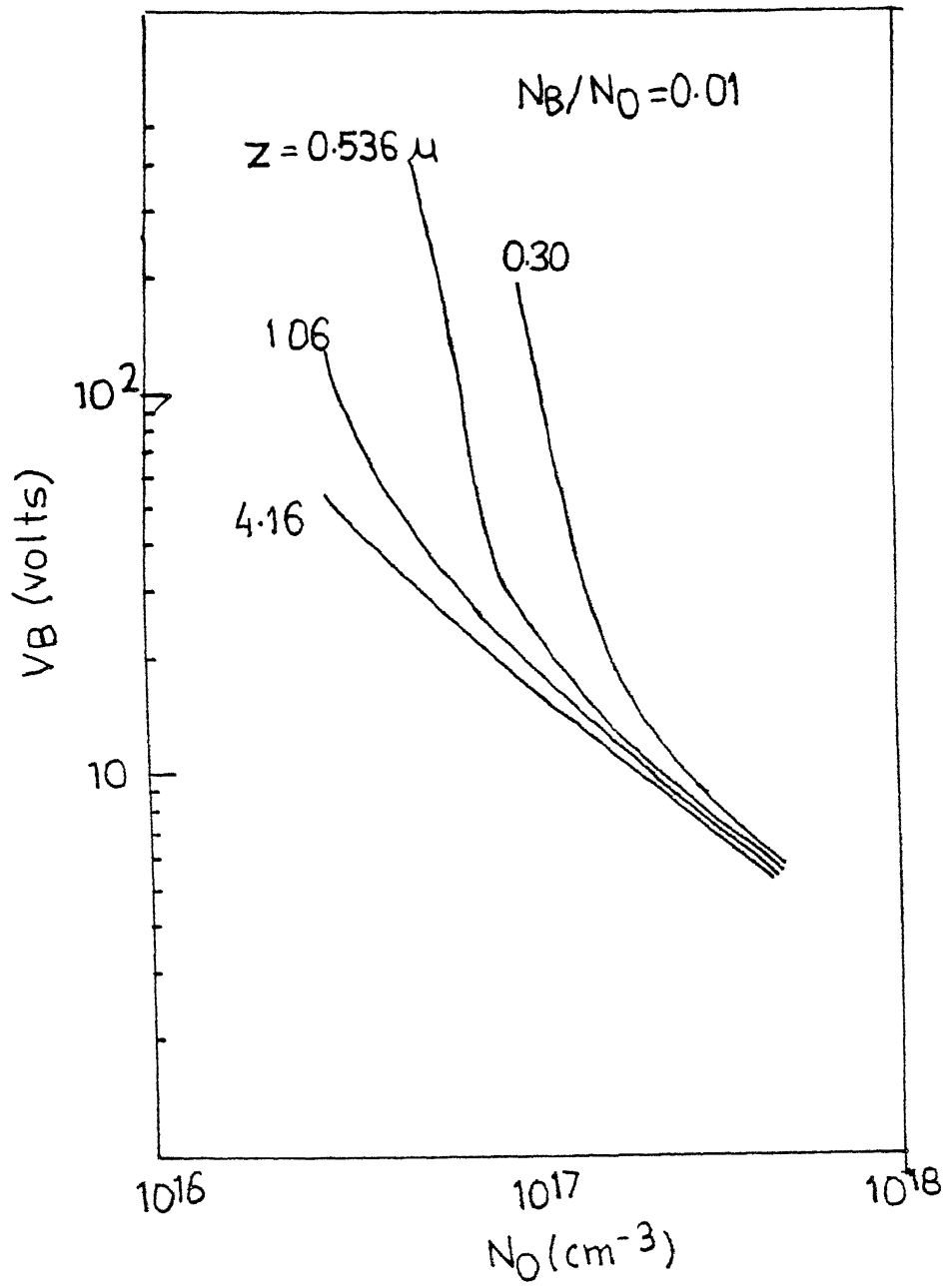
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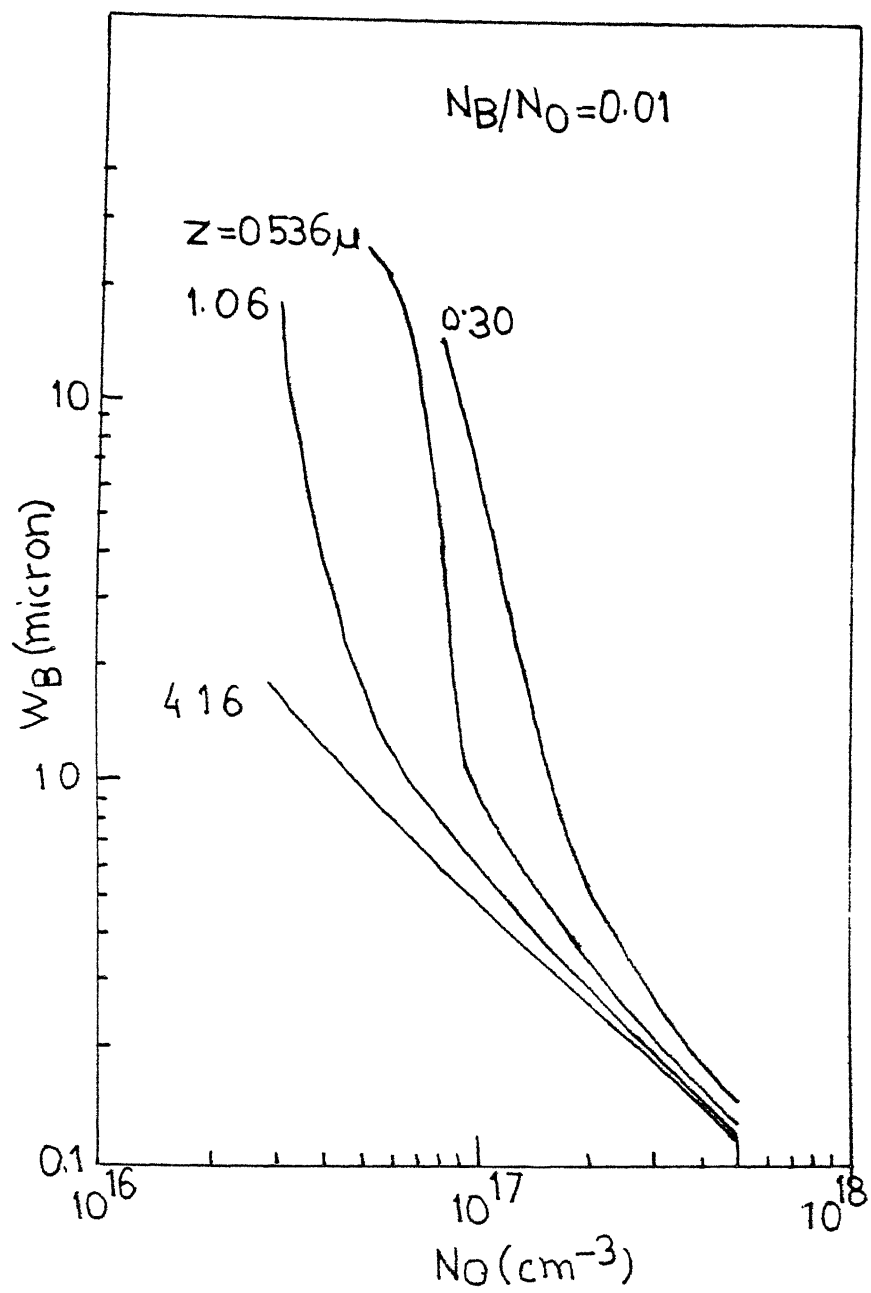
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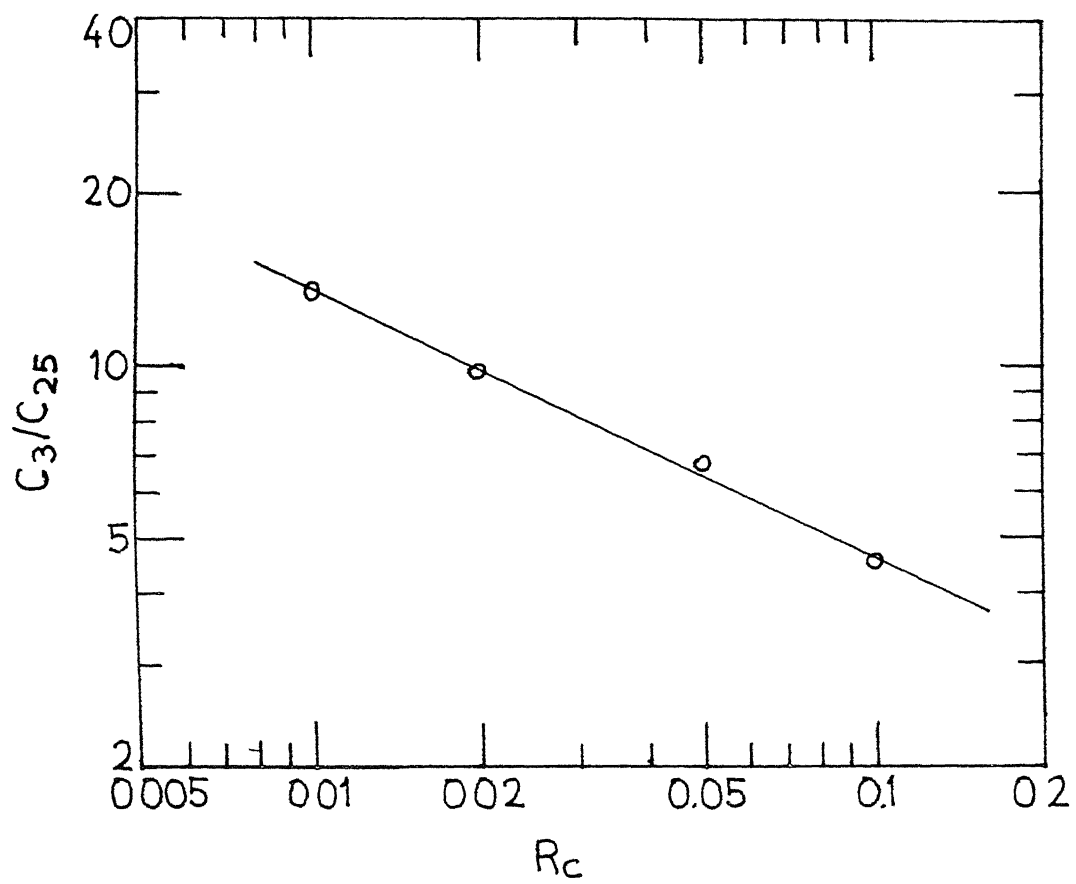
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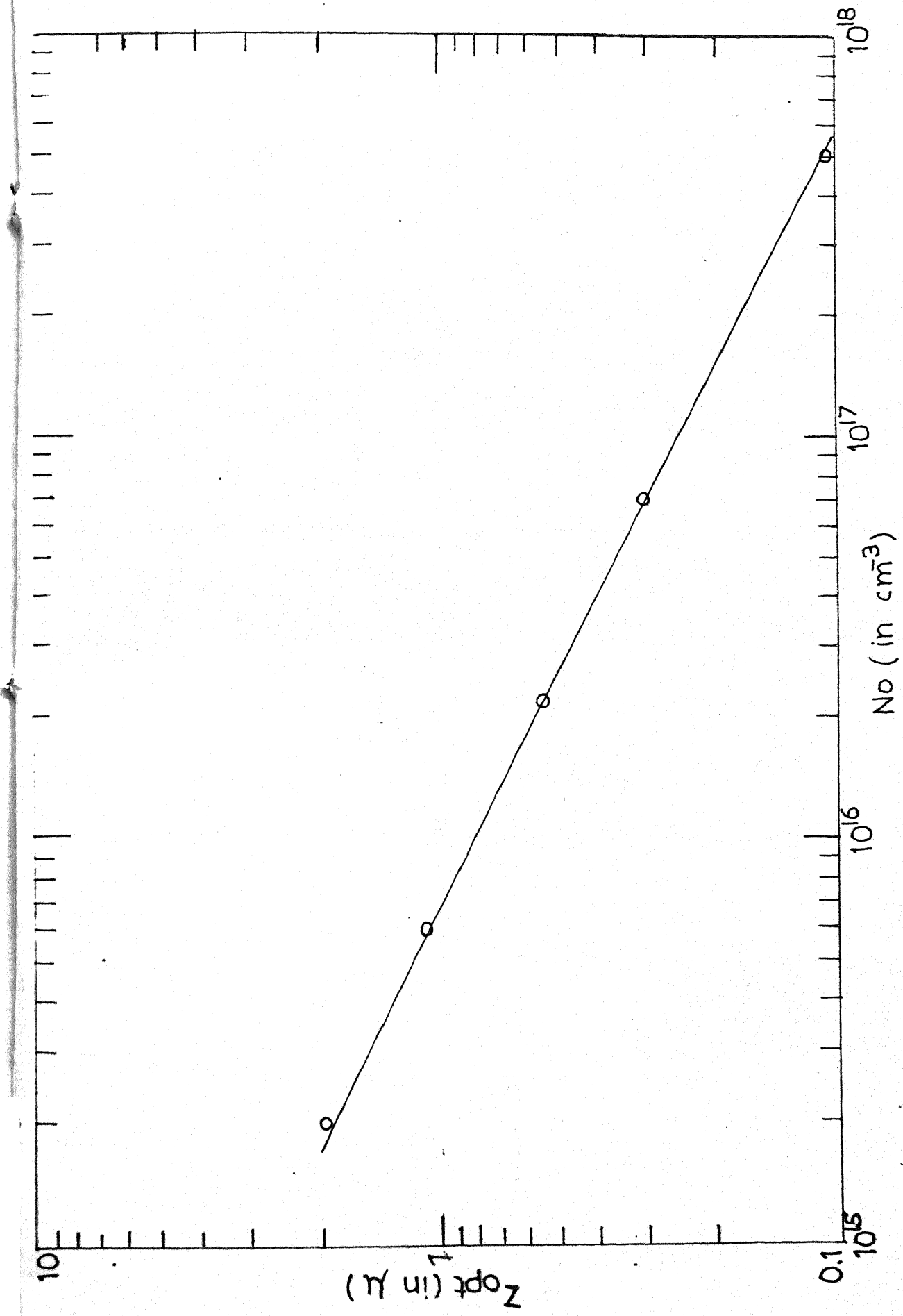
Fig. 8

Fig 9

Fig 10

Fig 11

98559

- NIG-DES